EPTC 2025 – Professional Development Courses (PDCs)

1. Advanced Substrates for Chiplets, Heterogeneous Integration, and Co-Packaged Optics

Speaker: John H Lau, Unimicron Technology Corporation

Course Objectives

Today, most of the package substrates for HPC driven by AI (artificial intelligence) are made by the 2.5D IC integration. In general, for 2.5D or CoWoS (chip on wafer on substrate), the SoC and high bandwidth memories (HBMs) are supported by a TSV-interposer and then solder bump and underfill on a build-up package substrate. However, because of the ever-increasing size of the TSV-interposer, the manufacture yield loss of the TSV-interposer is becoming unbearable. The key players such as NVIDIA, AMD, Intel, SK Hynix, Samsung, Micron, TSMC, etc. are working very hard to eliminate the TSV interposer and put the HBMs directly on top of the SoC (3.3D IC integration). Front-end integration of some of the chiplets (before package heterogeneous integration) can yield a smaller package size and a better performance (3.5D IC integration). In the past few years, 2.3D IC integration or CoWoS-R is getting lots of traction. The motivation is to replace the TSV-interposer with a fan out fine metal L/S redistribution-layer (RDL)-substrate (or organic-interposer). In general, for 2.3D, the package substrate structure (hybrid substrate) consists of a build-up package substrate, solder joints with underfill, and the organic-interposer. Today, 2.3D is already in production. Recently, TSMC published two papers on replacing the large-size TSV-interposer by LSIs (local silicon interconnects, i.e. Si bridges) and embedding the LSIs in fan-out RDL-substrate. TSMC called it CoWoS-L. Recently, since Intel's announcement on the glass core substrate for their one-trillion transistors to be shipped before 2030, glass core substrate has been a very hot topic. Since the shipments of co-packaged optics (CPO) by Intel and Broadcom CPO have been getting lots of tractions. In this lecture, the introduction, recent advances, and trends in the substrates of 3.5D IC integration, 3.3D IC integration, 3D IC integration, 2.5D IC integration, 2.3D IC integration, 2.1D IC integration, 2D IC integration, fan-out RDL, embedded Si-bridge, CoWoS-R, CoWoS-L, CPO, and glass core for HPC driven by AI will be discussed. Some recommendations will be provided.

Course Outline

Introduction

Substrate Definition

Substrates for Chiplet and Heterogeneous Integration

2D IC Integration

2.1D IC Integration

2.3D IC Integration

2.5D IC Integration

3D IC Integration

3.3D IC Integration

3.5D IC Integration

Bridges Embedded in Build-up Substrates

Bridges Embedded in Fan-Out EMC with RDLs

Glass-Core Build-up Substrates and TGV-Interposers

CPO Substrates

Summary and Recommendations

Lecturer Bio

John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 535 peer-reviewed papers (385 are the principal investigator), 52 issued and pending US patents (31 are the principal inventor), and 24 textbooks (all are the first author). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

Photo:


(online)

Who Should Attend?

If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. The lectures are based on the publications by many distinguish authors and the books (by the lecturer).

2. Photonic Components and Packaging Technologies for Data Center, Communication, Sensing, and Displays

Speaker: Torsten Wipiejewski, Huawei Technologies

Course Objective:

This course will provide an overview on the various photonic components and packaging technologies that enable optical interconnects, communication, sensing, and modern display applications. These applications are key for the information and communication technology of today and path a way to the future. High speed optical interconnects from board level in data centers to long haul transmission systems requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of various types including VCSELs, high speed optical modulators and photodetectors.

AI has become a major driver to increase data throughput in data centers and high-performance computing. Optical interconnects offer a large bandwidth and can help to reduce energy consumption for data transfer. Bringing the optical engine close to the GPU/ASIC core is the target of co-packaged optics (CPO) solutions replacing the electrical signal lines on board level. Packaging technologies play a key role in the implementation of optical solutions, because the cost of the system is typically dominated by the assembly and packaging cost. Integration schemes such as photonic integrated circuits PICs have become mainstream technologies for cost and size reduction. Therefore we will discuss optical waveguides and the coupling of optical waveguides and components to optical fibers. This is a key challenge in optical packaging because of the tight alignment tolerances.

Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitates the usage by end-users without specific medical knowledge. Displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops and tablets all the way to large screen TVs and video walls. We review current technologies and new developments such as quantum dots and micro LEDs as well as some features of 3D displays. In particular, micro LEDs for large size displays require novel assembly technologies to mount chips of only several micro

meter in size with extremely high yield at very low cost. The mass transfer of thousands of chips simultaneously is an option to achieve this challenging target.

Course Outline:

- Fundamental properties of photonic components
- Light sources: LEDs, laser diodes, VCSELs, others
- Transmitter and receiver components in optical data communication systems: lasers, modulators, photodetectors, passive optical components, optical modules, co-packaged optics (CPO)
- Monolithic and hybrid integration, photonic integrated circuits PICs, silicon photonics, optical waveguides and optical fiber coupling, assembly and packaging.
- Optical sensing elements and applications: spectrometers, light sources, photoacoustic sensors, frequency combs
- Display technologies: liquid crystal displays LCD, organic light emitting diode OLED displays, quantum dot emissive layers, micro LED arrays and large size displays using chiplet mass transfer and bonding, 3D displays
- Summary and outlook

Lecturer Bio:

Dr. Torsten Wipiejewski joined Huawei Technologies in 2014 and is responsible for the European technology sourcing of Huawei's Hardware Engineering Institute. His interest covers all hardware aspects for products ranging from smart watches to optical communication systems. He has also been appointed as Technical Advisor to the President of Huawei's European Research Institute. Previously, Torsten was an investor in renewable energy, CEO at Optogan (Germany, Finland) making blue LEDs, and COO at Firecomms (Ireland) making optical transceivers for automotive applications. He also held management positions at ASTRI in Hong Kong, Agility Communications in Santa Barbara, CA, USA as well as Infineon, Osram, and Siemens in Germany. Torsten received a "summa cum laude" Ph.D. degree in electrical engineering from the University of Ulm, Germany and has been an executive member of several international conferences. He was the General Chair of ECTC 2008 and has lectured several courses at conferences and universities. He holds more than 30 patents and has published over 100 scientific papers and presentations.

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Who Should Attend:

The course addresses engineers, scientists and students who would like to get a general overview of various photonics technologies used in todays products and future developments. The aim is to describe which photonic technologies can be used in various applications and what current limitations are and which new technologies are being developed for further improvements or aiming at technology break throughs.

3. Advanced Packaging for MEMS and Sensors

Speaker: Horst Theuss, Infineon Technologies AG

Course Objectives

Sensors are everywhere! They create data and provide the “food” for the Internet of Things.

Which specific requirements distinguish MEMS and sensor packaging from standard assembly? How are these challenges being tackled? Do we need advanced packaging technologies for MEMS? These are just a few questions which are addressed in the course.

From a general introduction into package platforms, MEMS-specific challenges will be derived – e. g. the need for low package induced stress and its impact to MEMS performance, the necessity to create cavities or the implementation of MEMS-specific package materials and processes. The course reviews the state of the art, but also explores some topics in more detail. These topics refer to case studies comprising pressure and impact sensors, microphones, mirrors, magnetic sensors, and Radar devices. A further section elaborates on robustness requirements and approaches for risk mitigation in harsh environments.

A discussion on advanced packaging contains developmental studies on integrating MEMS-microphones or RF-antennas into Fan-Out-Wafer-Level-Packages.

The concluding chapter deals with systems and heterogeneous integration. Where is the overlap of the processor-driven world of advanced packaging and the MEMS/Sensor world? Where are differences, how can we overcome them and where will the future lead us?

Lecturer Bio:

Horst Theuss received his Ph.D. degree in Physics from the University of Stuttgart, Germany in 1993. His research was awarded a “Otto Hahn Medal for Young Scientists” by the Max Planck Society. As a research staff member at the Max Planck Institute for Metal Research he concentrated on magnetic properties of superconductors and amorphous materials. Within a post-doctoral assignment at the IBM Almaden Research Center in San Jose, CA, he worked on magneto-optical properties of exchange-coupled

thin layers. In 1996, he started his industrial career at Vacuumschmelze GmbH, Hanau/Germany as a product marketing manager for alloys with special magnetic properties. Horst Theuss joined Infineon Technologies, Regensburg, Germany in 2000. Since then he has been developing package concepts and processes in the fields of discrete semiconductors, wafer level packaging, cavity packaging, materials and system integration. As a Senior Principal he is today responsible for predevelopments with a focus on MEMS and sensors. Over the years, Horst has continuously contributed to a variety of conferences and magazines with presentations, papers and seminars. He holds more than 100 patents and is co-editor of the “Handbook of Silicon based MEMS Materials and Technologies”. Horst gives regular lectures on Advanced Packaging at the University of Applied Science in Regensburg, Germany.
Photo: (Provided by Speaker)

Who should attend?

The course is intended for engineers and technical managers working in the field of MEMS or sensors. It gives an overview on the MEMS packaging landscape but also elaborates more fundamentally into selected topics. It will as well welcome students and newcomers, who are interested to broaden their MEMS-specific knowledge.

4. Overview of Characterization Techniques for 3D Heterogeneously Integrated Circuit Packaging

Speaker: Dr Ali Shakouri, Purdue University

Abstract of PDC

An overview of structural, mechanical, and thermal characterization techniques for advanced integrated circuits and 3D heterogeneously packaged chips will be given. This includes characterization of thin film materials and interfaces in complex ICs. Optical inspection, X-ray computed tomography, scanning acoustic microscopy, and optical pump-probe imaging are used for passive IC packages. Thermal imaging, deformation/stress analysis, and magnetic current imaging are performed on active ICs during operation. Key focus will be on the buried structures and 3D geometries. As feature sizes decrease, an overview of emerging ultrasonic and scanning probe techniques will also be presented. We highlight challenges in extracting key material and interface physical parameters, identifying buried defects, and the limits in spatial resolution and measurement times. Wafer-scale characterization of bonding interfaces, multi-layer interconnects, multi-chip modules, and through-silicon vias is particularly challenging, and rapid scanning techniques will be highlighted.

Lecturer Bio

Dr Ali Shakouri is an electrical and computer engineering professor and associate dean of research and innovation at Purdue College of Engineering. He received his Diplome d'Ingenieur in 1990 from Telecom Paris, France, and his Ph.D. in 1995 from the California Institute of Technology. He was a faculty at the University of California in Santa Cruz before moving to Purdue in 2011 to lead the Birck Nanotechnology Center for ten years. He has worked extensively in nanoscale heat transport and electrothermal energy conversion. His group has developed and commercialized a novel lock-in imaging technique to obtain thermal maps of integrated circuits and active devices with submicron spatial and nanosecond time resolution. At the Birck Center, he led the SMART consortium focused on low-cost printed sensors and IoT networks to expand the collaboration between engineering, agriculture, pharmacy, and veterinary medicine. He currently leads an NSF Future Manufacturing project with colleagues at Purdue, Harvard,

and Tuskegee University focused on deploying artificial intelligence techniques in small and medium manufacturers.

Photo (found online)

Who Should Attend

This course is designed for engineers, researchers, and students involved in structural, thermal, and materials characterization of advanced ICs and 3D heterogeneously integrated packages. It is especially relevant for those working on failure analysis, interface evaluation, and high-resolution inspection of buried structures, thin films, and wafer-scale interconnects.